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Implementation of Various Logic Circuits and Evaluation by Power Efficiency

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Abstract: *The power dissipation in standard CMOS circuit can be decreased through adiabatic technique. By adiabatic technique dissipation in PMOS network may bedecreased and a few of energy keep at load capacitance may be recycled rather than dissipated as heat. however the adiabatic technique is extremely passionate about parameter variation. With the assistance of MICROWIND simulations, the energy consumption is analyzed by variation of parameter. In analysis, 2 logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback adiabatic Logic) area unitcompared with standard CMOS logic for electrical converter NAND and NOR circuits. it's finding that adiabatic technique is sweet alternative for low power application in nominative frequency vary.*

Keywords: *Power Consumption in CMOS , Equivalent Circuits, Four Phased Power Clock, Adiabatic Technique.*

I. Introduction

The term "adiabatic" describe the physical science processes within which no energy exchange with the atmosphere, and so no dissipated energy loss. However in VLSI, the electrical charge transfer between nodes of a circuit is taken into account because the method and numerous techniques may be applied to reduce the energy loss throughout charge transfer event. Absolutely adiabatic operation of a circuit is a perfect condition. It's going tobe solely achieved with terribly slow change speed. In sensible cases, energy dissipation with a charge transfer event consists of an adiabatic element and a non-adiabatic element. In standard CMOS logic circuits, from zero to VDD transition of the output node, the full output energy drawn from power offer and keep in electrical phenomenon network. adiabaticlogic circuits scale back the energy dissipation throughout change method, and utilize this energy by utilization from the load capacitance. For utilization, the adiabatic circuits use the constant current supply power offer and for scale back dissipation it uses the tetragon or curving power offer voltage. The equivalent circuit won't to model the standard CMOS circuits throughout charging method of the output load capacitance. However here constant voltage supply is replaced with the constant current supply to charge and discharge the output load capacitance. thus adiabatic change technique offers the less energy dissipation in PMOS network and reuses the keep energy within the output load capacitance by reversing the present supply. Adiabatic Logic doesn't dead switch from zero to VDD (and vice versa), however a voltage ramp is employed to charge and recover the energy from the output. adiabatic circuits area unitlow power circuits that use "reversible logic" to conserve energy. whereas this is often a district of active analysis, current techniques believe heavily on transmission gates and four-phased tetragon clocks to attain this goal.

II. Proposed Method

CMOSLogicalFamilies:
Thetypesoflogiccircuitsare

- CMOSINVERTER
- CMOSNAND
- CMOSNOR

A. CMOSInverter

ThemostimportantCMOSgatelogicistheCMOSinverter.Itconsistsof solely 2 transistors,a try of1 N-typeandoneP-
type semiconductorunit.Asfig.1shows theessential circuitofCMOS electricalconverter.Voltagelevels areau nitatlogical'1' equivalentto electricallevelVCC,alogical'0'(correspondingto0VorGND).

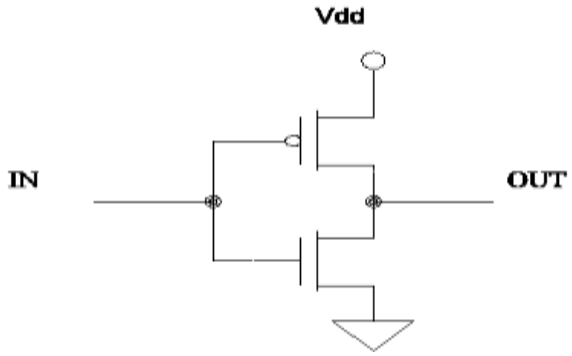

Fig1: CMO Sinvereter

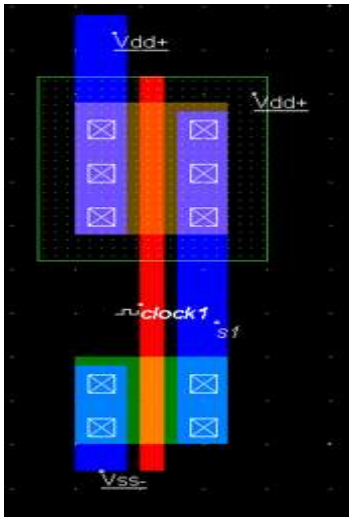

Fig.2: Layout Design of CMOS Inverter

Thelayout style ofCMOS inverter isdrawn inkeepingwith itscircuitdiagramasshowninfig.2.Here,PMOSisinbrowncolor,NMOSisin inexperienced color,themetal1through that they're connectedisblueincolor .Theredcolorshowspolysiliconlayer that isemployed togrant input.

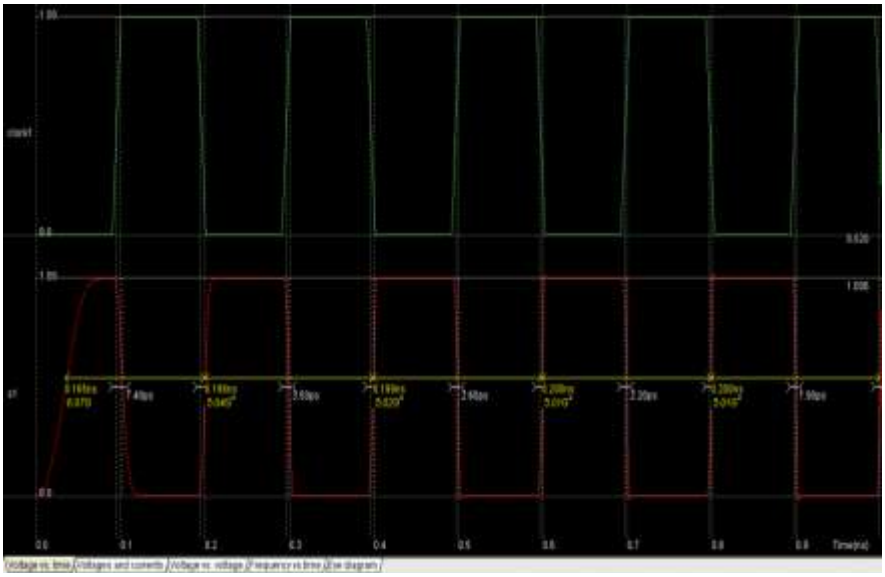

Fig.3: SimulationWaveformofCMOSInverter

In this simulation wave shape, it's noted that once input is 'High' the corresponding output is 'low'. CMOS NAND Circuit: A logic gate (Negated AND or NOT AND) may be a gate that produces AN output that's false provided that all its inputs area unit true. an occasional (0) output results provided that each the inputs to the gate area unit HIGH (1); if one or each inputs area unit LOW (0), a HIGH (1) output results. The logic gate is critical as a result of any Boolean perform may be enforcedby employing a combination of NAND gates. This property is named purposefulcompleteness.

B. CMOSNANDCircuit:

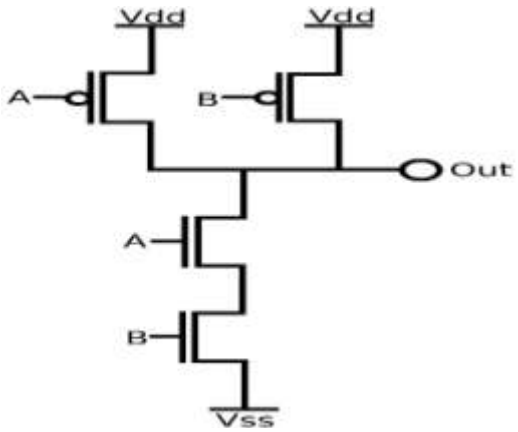

Fig.4:CMOSNANDGateCircuit

InCMOSNANDcircuit,PMOSareconnectedinparallelandNMOSareconnectedinseries.

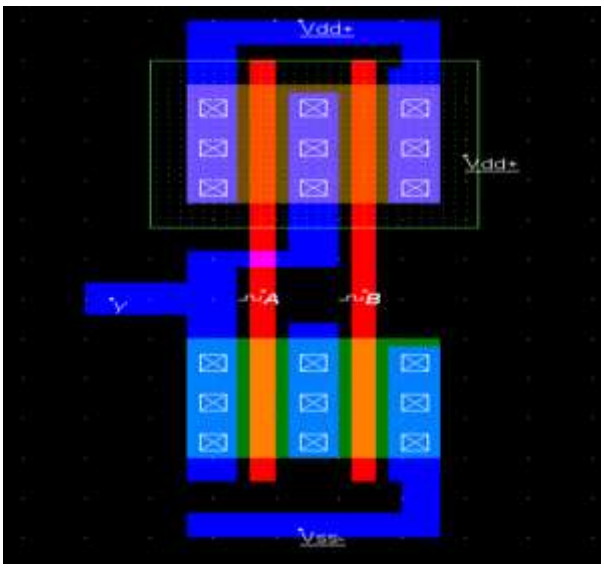

Fig.5: LayoutofCMOSNANDGate

ThelayoutdesignofCMOSNANDgateisdrawnaccordingtoitscircuitdiagramasshowninFig.4.Inthetwo-input,NANDgatetheP-typetransistorsareconnectedinparallelbetweenVCCandtheoutput,andtheN-typetransistorsareconnectedinseriesfromVsstotheoutput.

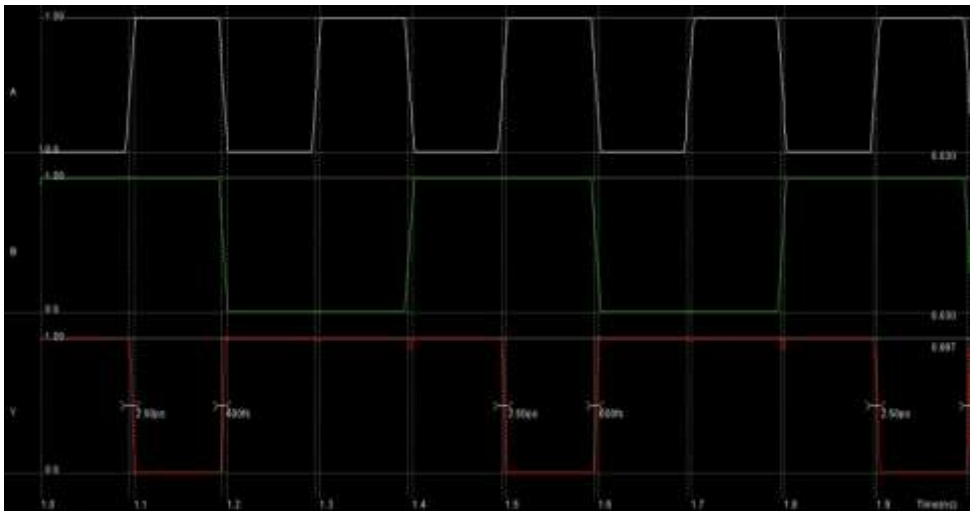

Fig.6: SimulationWaveformofCMOSNANDGate

InthesimulationwaveformofCMOSNANDgate,itisseenthatwhenbothinputsareat'High',thecorresponding outputis'Low'andviceversa.

C. CMOSNORCircuit:

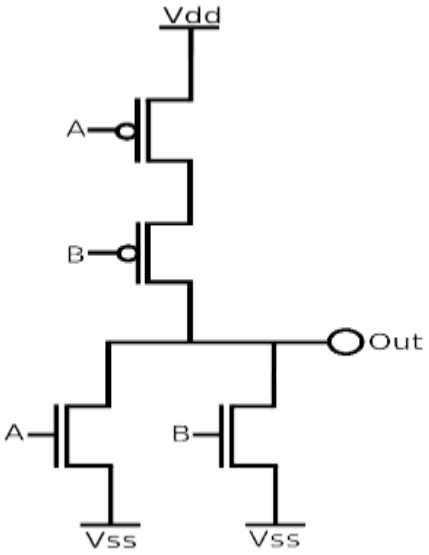

Fig.7:CMOSNORgatecircuits

TheNORgate maybea digital gate thatimplementslogicalNOR-
itbehaves inkeepingwith thereality tableto theproper.AHIGHoutput(1)resultsif each theinputstothegate are aunit LOW(0);ifoneor each inputisHIGH(1), anoccasionaloutput(0)results. neitheris the resultsofthenegati onoftheORoperator.It caneven beseenas AN ANDgate withalltheinputsinverted. neitheris a performallyco mpleteoperation—
combinationsofNORgates maybe combined toget theotherlogicalfunction. againstthis,theORoperatorismo notonic becauseit will solelymodification LOWtoHIGH however not contrariwise.Thelayout style ofCMO S neitheris drawn inkeepingwith itscircuitdiagramasshowninfig.7. withinthe two-inputNORgatetheP-typetransistors areaunit connected asynchronous betweenVCC andalsothe output, whereas theN-typetransistors areaunit connectedinparallelfromGNDtotheoutputY.

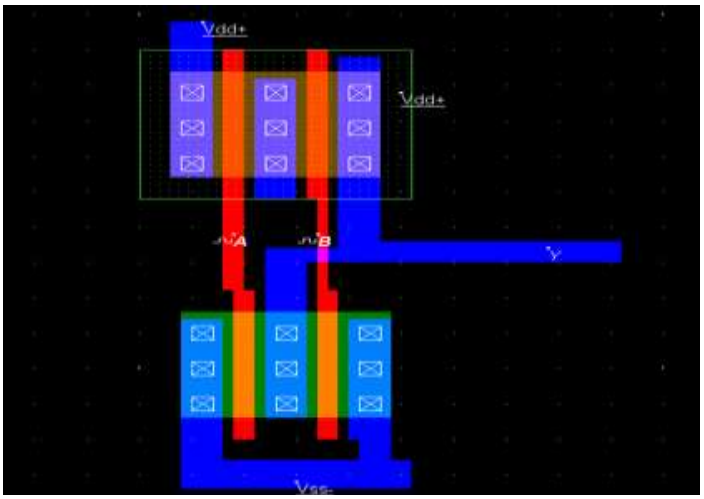

Fig.8: LayoutDesignofCMOSNORGate

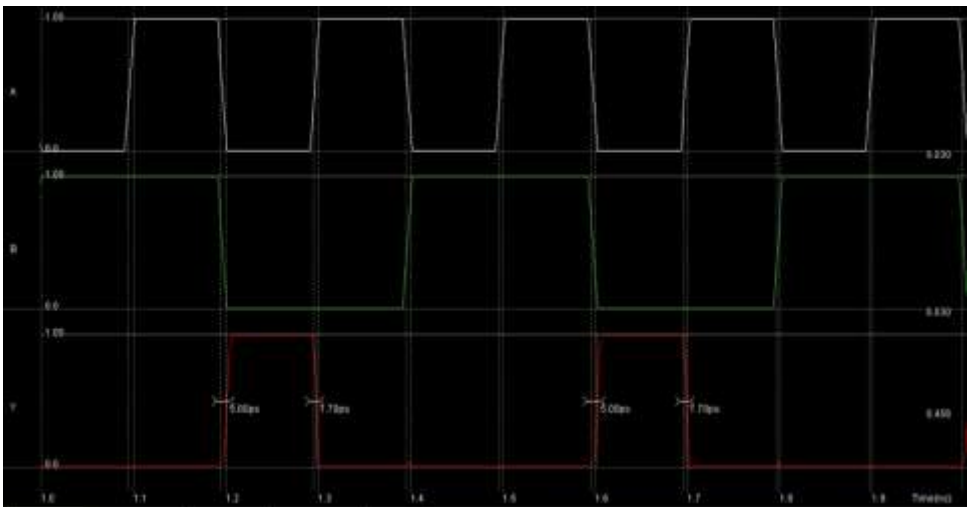

Fig.9: SimulationWaveformofCMOSNORGate

D. CMOSANDcircuit:

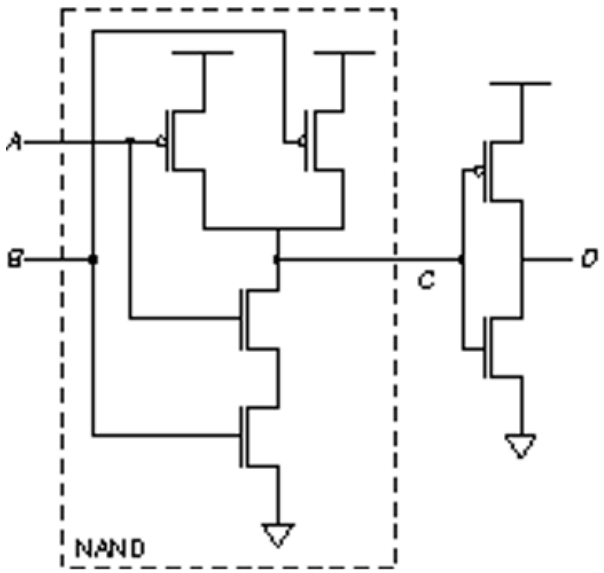

Fig.10:CMOSANDcircuit

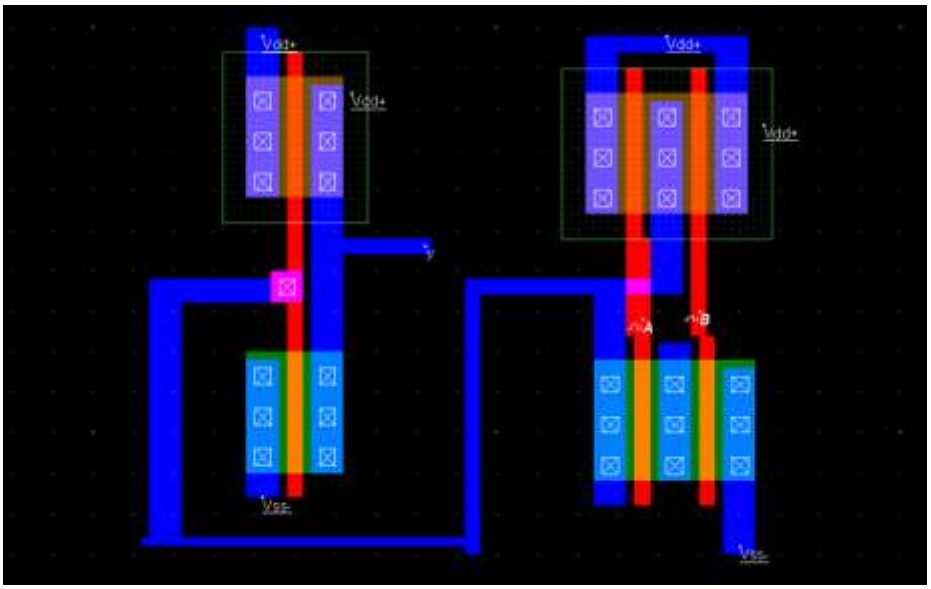

Fig.11: LayoutDesignofCMOSANDGate

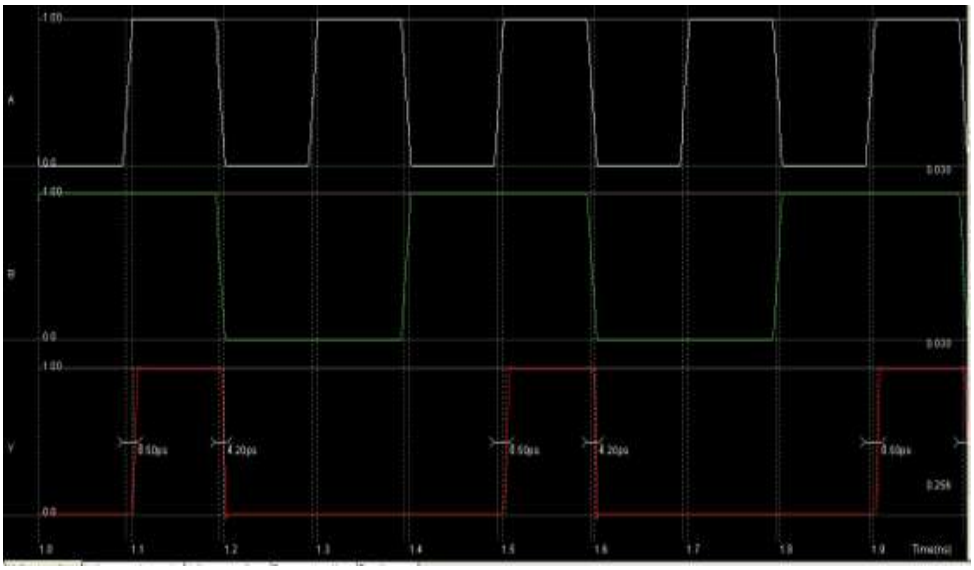

Fig.11: SimulationWaveformofCMOSNORGate

E. CMOSORcircuit

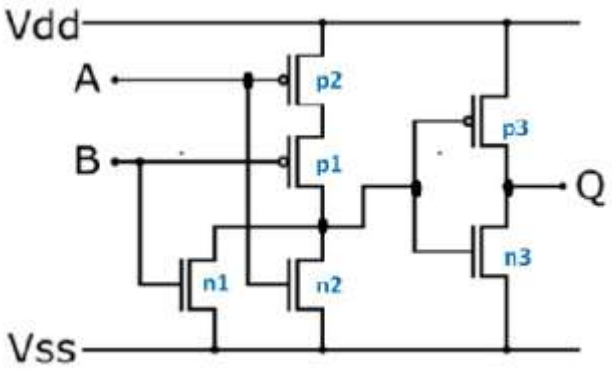

Fig.12:CMOSORcircuit

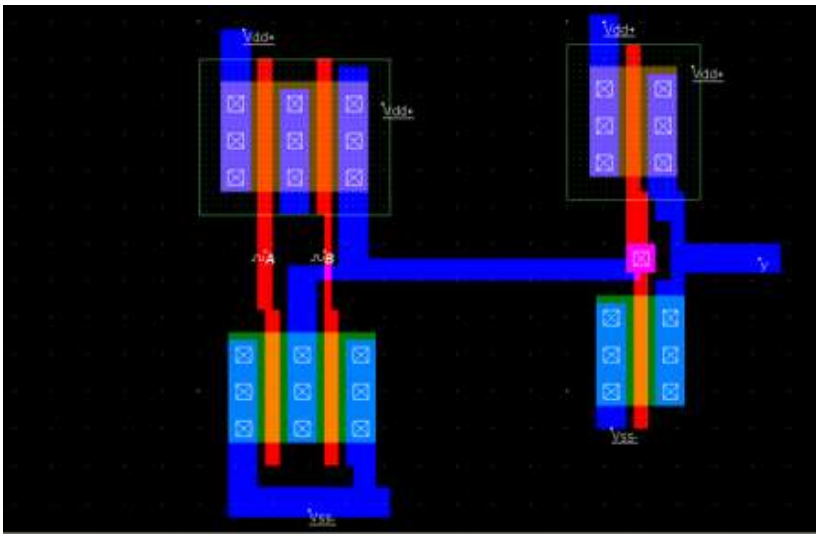

Fig.13: LayoutdesignofCMOSORcircuit

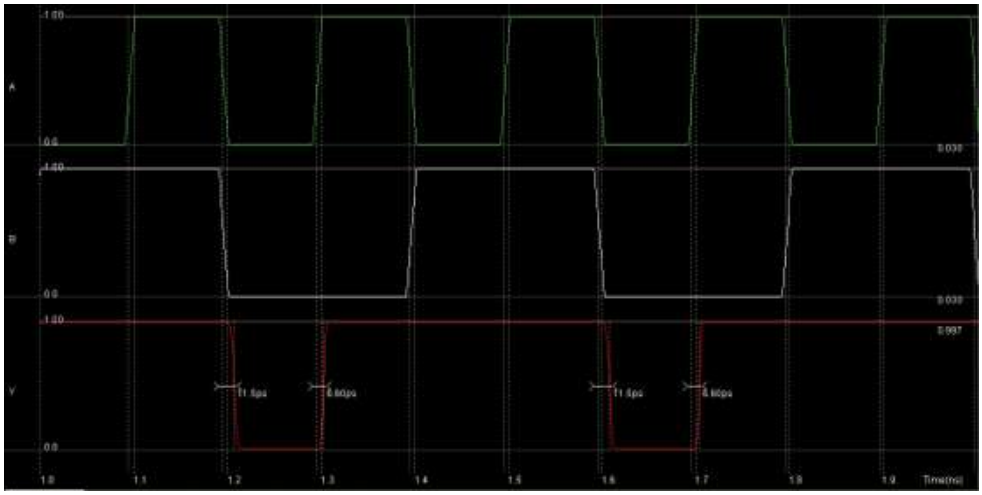

Fig.14: SimulationwaveformofCMOSORgate

III. Conlusion

Thedifferentparametervariationsagainst cmos logicfamilies areaunitinvestigated, that showsthat c moslogicfamilies extremely dependon itsparametervariations. however lessenergyconsumptionin cmos lo gicfamilies maybe stillachievedwiththehelpofthe bigselection ofparametervariations.NANDandNORcircui tsshows higher energysavingsthanANDandORatthehighfrequencyandhighloadcapacitance. Duetomoretrasi storarepresentinCMOSAND,CMOSORcircuitspowerconsumptionismoreinthatcircuitoverCMOSNAND,C MOSNORgatecircuits.

IV. FutureWork

- Infuture,adiabaticlogicaretobeintroducedwhichcanhelpinovercomingthedisadvantagesofconventionalCMOS logiccircuits.Forexample-DFAL(DiodeFreeAdiabaticLogicCircuit).
- ForexamplewewillimplementINVERTER,NAND,NOR,AND,ORadiabticlogiccircuits
- Studyofcomparisonofadiabaticlogicsconnectedwithdifferenttypesofmultipliersindifferentparametersmayalso bedoneinfuture.
- Futureworkalsoincludesthedesignoflargeradiabaticgatesandcircuitfromtheproposedbuffer/inverteranddissipa tedenergyanalysisathigherfrequenciesandcomparisonwithotheradiabaticfamilies.

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